# SP8853

## 1.3 GHz Professional Synthesiser
## Data Sheet

June 2003

The SP8853 is a low power single chip synthesiser intended for professional radio applications, containing all the elements (apart from the loop amplifier) required to build a PLL frequency synthesis loop

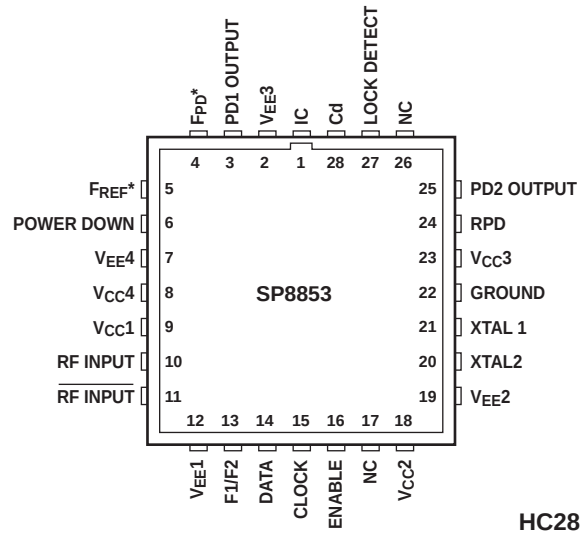
The device is serially programmable by a three-wire data highway and contains three independent buffers to store one reference divider word and two local oscillator divider words. A digital phase detector with two charge pumps, programmable in phase and gain, are provided to improve lock-up performance. The preset operation of the charge pumps can be overwritten or the comparison frequencies switched to output ports under control of the divider word. The dual modulus ratio and so operating range is also programmable through the same word.

A power down mode is incorporated as a battery economy feature.

The SP8853 is specified at 1.3GHz at -55°C to +125°C (mil temp) and -40°C to +85°C (ind. temp).

### FEATURES

- Improved Digital Phase Detector Eliminates 'Dead Band' Effects
- Low Operating Power, Typically 175mW
- 1·3GHz Operating Frequency
- Complete Phase Locked Loop
- High Input Sensitivity
- Programmed throughThree-Wire Bus
- Wide Range of Reference Division Ratios
- Local Storage for Two Frequency Words, giving Rapid Frequency Toggling
- Programmable Phase Detector Gain
- Power Down Mode




*$F_{PD}$ and $F_{REF}$ outputs are reversed by the phase detector sense bit in the F1/F2 programming word. The above diagram is correct when the sense bit is low. See Table 2 and Fig. 7.

$V_{CC}1$, $V_{EE}1$ – preamplifier and prescaler supplies
$V_{CC}2$, $V_{EE}2$ – oscillator supplies
$V_{CC}3$, $V_{EE}3$ – charge pump 2 supplies
$V_{CC}4$, $V_{EE}4$ – ECL supplies

*Fig. 1 Pin identification diagram (top view)*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | −0·3V to +7V |
| Storage temperature | −55°C to +150°C |
| Prescaler input voltage | 2·5V p-p |

### ORDERING INFORMATION

**SP8853/A/DG, SP8853/A/HC Industrial temperature versions**
**SP8853/AC/DG, SP8853/AC/HC Military temperature versions**

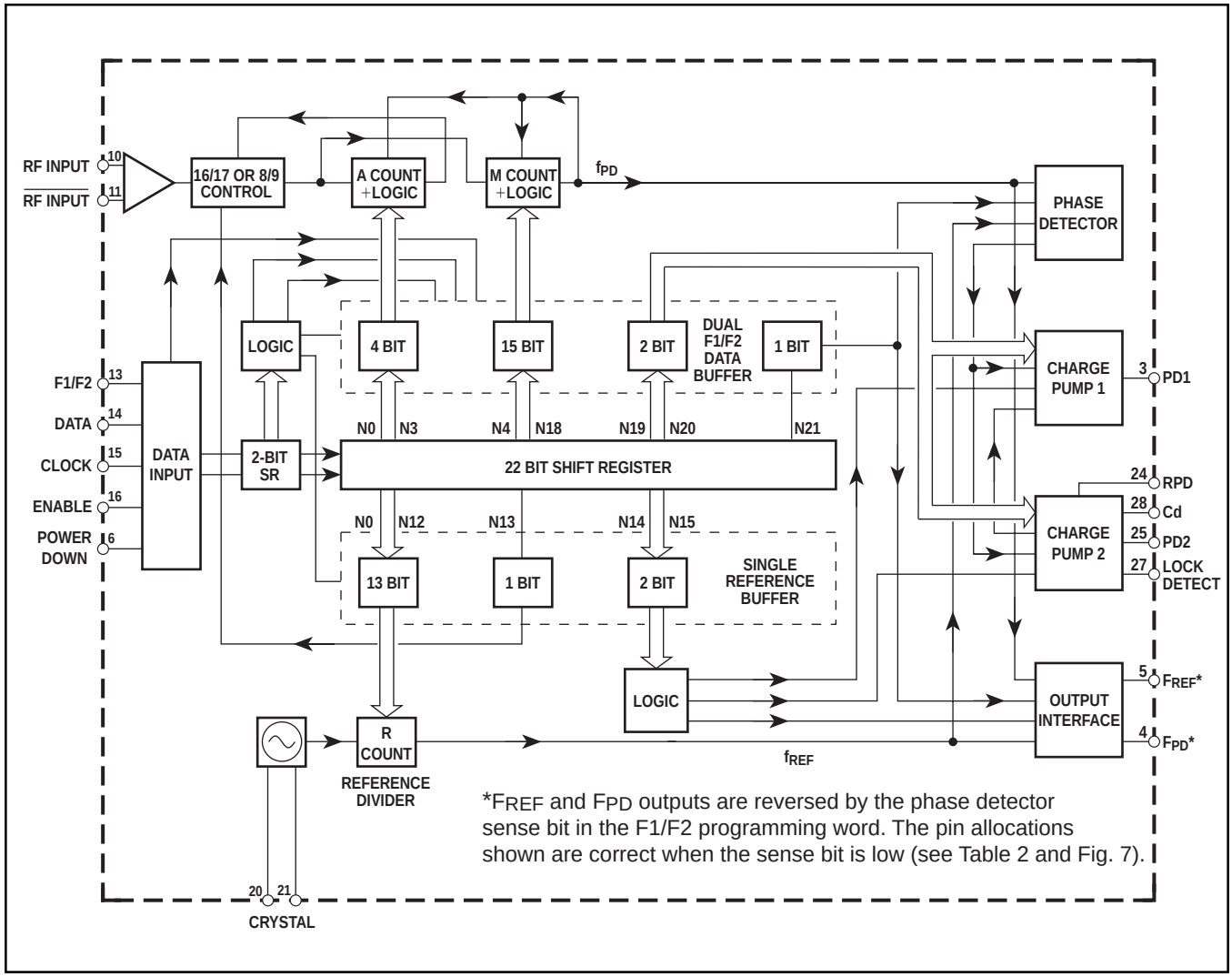



*Fig. 2 SP8853 block diagram*

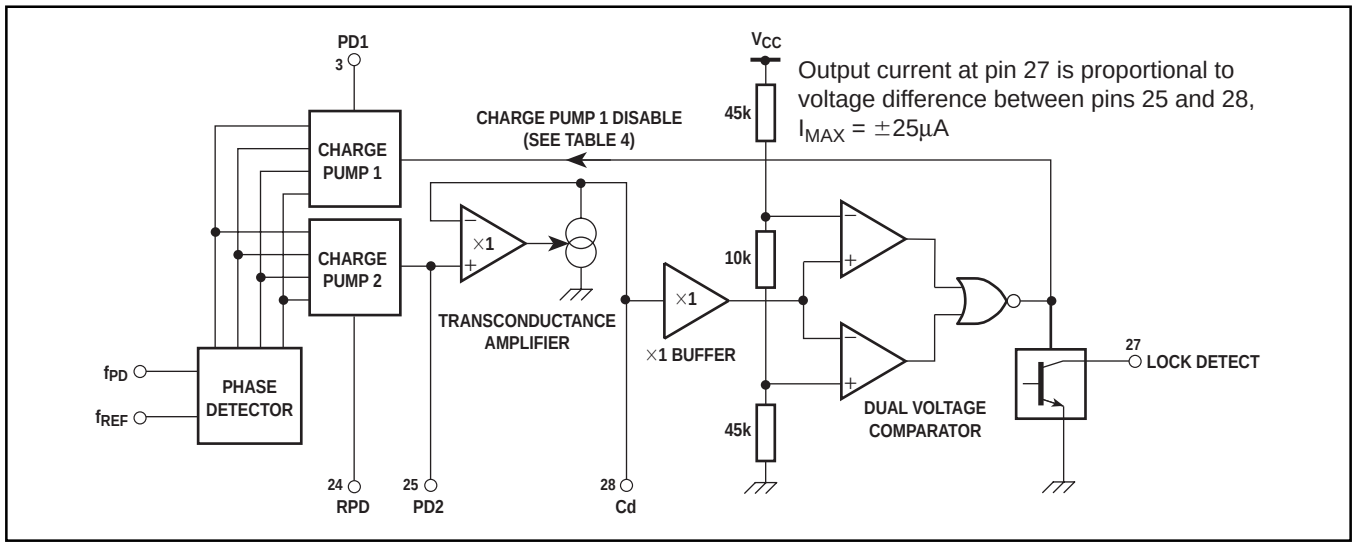



*Fig. 3 Detailed block diagram of lock detect circuit*

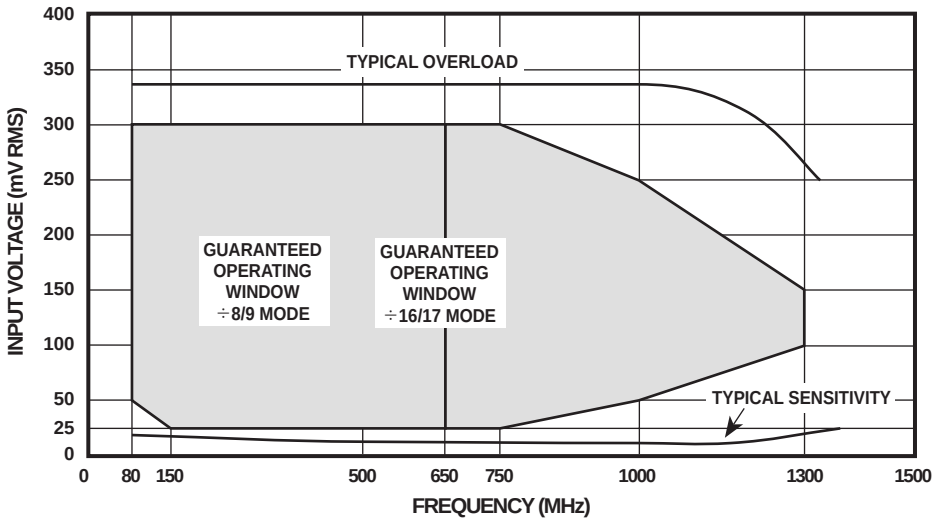
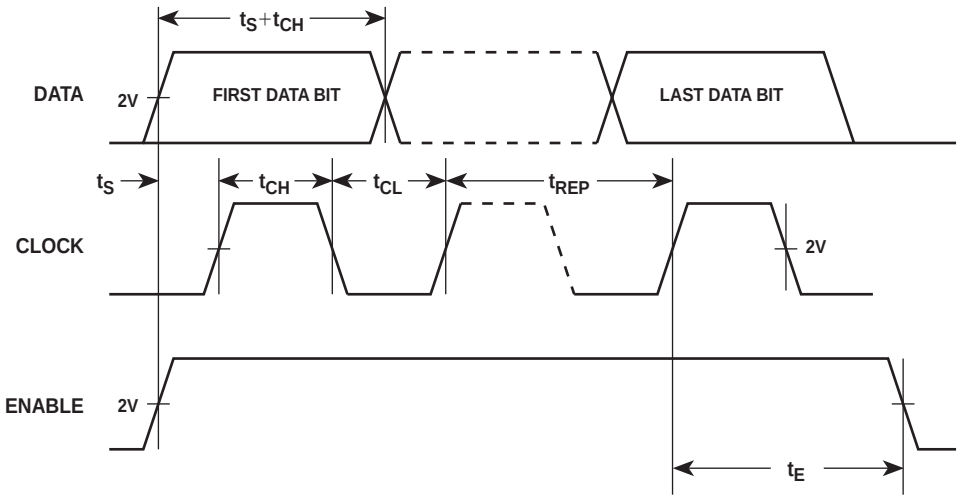



*Fig. 4 Typical input characteristics and input drive requirements for SP8853 A and B*




$t_{REP}$ = 1µs min., $t_S$ = 50ns min., $t_{CH}$ = 50ns min., $t_{CL}$ = 100ns min., $t_E$ = 50ns min.

*Fig. 5 Data and clock timing requirements*

## ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following range of operating conditions unless otherwise stated:
Supply voltage $V_{CC}$ = +4·75V to +5·25V. $T_{AMB}$ = −55°C to +125°C (A Grade), −40°C to +85°C (B Grade)

| Characteristic | Pin | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply current | 8,9,18,23 | | 33 | 40 | mA | |
| Supply current in power down mode | 8 | | 4·5 | 7·5 | mA | |
| Input sensitivity | 10,11 | | | | | See Fig. 4 |
| Input overload | 10,11 | | | | | See Fig. 4 |
| RF input division ratio | 10,11,4 | 256 | | 524287 | | With ÷16/17 selected |
| | | 56 | | 262143 | | With ÷8/9 selected |
| Comparison frequency | 4,5 | | | 5 | MHz | |
| Reference oscillator input frequency | 20,21 | 4 | | 20 | MHz | |
| External reference input voltage | 20 | 10 | | 500 | mVrms | |
| Reference division ratio | 20,5 | 1 | | 8191 | | |
| Data clock repetition rate, $t_{REP}$ | 15 | | | 1 | µs | See Fig. 5 |
| Minimum setup time, $t_S$ | 14,15 | 50 | | | ns | See Fig. 5 |
| DATA input high | 14 | $0{\cdot}6V_{CC}$ | | $V_{CC}$ | V | |
| DATA input low | 14 | $V_{EE}$ | | $0{\cdot}3V_{CC}$ | V | |
| CLOCK input high | 15 | $0{\cdot}6V_{CC}$ | | $V_{CC}$ | V | |
| CLOCK input low | 15 | $V_{EE}$ | | $0{\cdot}3V_{CC}$ | V | |
| Data ENABLE high | 16 | $0{\cdot}6V_{CC}$ | | $V_{CC}$ | V | |
| Data ENABLE low | 16 | $V_{EE}$ | | $0{\cdot}3V_{CC}$ | V | |
| F1/F2 input high | 13 | $0{\cdot}6V_{CC}$ | | $V_{CC}$ | V | F1 buffer selected |
| F1/F2 input low | 13 | $V_{EE}$ | | $0{\cdot}3V_{CC}$ | V | F2 buffer selected |
| POWER DOWN input high | 6 | $0{\cdot}6V_{CC}$ | | $0{\cdot}9V_{CC}$ | V | |
| POWER DOWN input low | 6 | $V_{EE}$ | | $0{\cdot}3V_{CC}$ | V | |
| F1/F2 input current | 13 | | | 5 | µA | V pin 13 = 5·0V |
| POWER DOWN input current | 6 | | | 5 | µA | V pin 6 = 4·5V |
| RDP external resistance | 24 | 68 | | 330 | kΩ | |
| LOCK DETECT output voltage when in lock | 27 | | | 1 | V | I pin 27 = 1mA |
| LOCKDETECT switching voltage high | 25 | 2·7 | | | V | $V_{CC}$ = 5V |
| LOCK DETECT switching voltage low | 25 | | | 2·3 | V | $V_{CC}$ = 5V |
| $F_{PD}$ and $F_{REF}$ output voltage swing | | | 0·9 | | V | $V_{CC}$ = 5V, external pulldown may be required |

## DESCRIPTION

### Prescaler and AM Counter

The programmable divider chain is of *AM* counter design and therefore contains a dual modulus front end prescaler, an *A* counter which controls the dual modulus ratio and an *M* counter which controls the bulk multi-modulus division. A programmable divider of this type has a division ratio of $MN+A$ and a minimum integer steppable division ratio of $N(N-1)$.

In the SP8853, the dual modulus front end prescaler is a dual *N* ratio device, capable of being statically switched between ÷16/17 and ÷8/9 ratios. The controlling *A* counter is of four-bit design, allowing a maximum count sequence of 15 ($2^4-1$), which begins with the start of the *M* counter sequence and stops when it has counted by the pre-loaded number of cycles. While the A counter is counting, the dual modulus prescaler is held in the $N+1$ mode then reverts to the *N* mode at the completion of the sequence.

The *M* counter is a 15-bit asynchronous divider which counts with a ratio set by a control word. In both *A* and *M* counters the controlling data from the F1/F2 buffer is loaded in sequence with every *M* count cycle. The *N* ratio of the dual modulus prescaler is selected by a one-bit word in the reference divider buffer and, when when a ratio of ÷8/9 is selected, the A counter requires only three programming bits, having an impact on the frequency bit allocation as described in the data entry section.

### Reference Source and Divider

The reference source in the SP8853 is obtained from an on-chip oscillator which is frequency controlled by an external crystal. The oscillator can also function as a buffer amplifier to allow the use of an external reference source. In this mode, the source is simply AC-coupled into the oscillator transistor base on pin 20.

The oscillator output is coupled to a programmable reference counter (*R*) whose output is the reference for the phase detector. The reference divider is a fully programmable 13-bit asynchronous design and can be set to any division ratio between 1 and 8191. The actual division ratio is controlled by a data word stored in the internal reference buffer.

### Phase Detector

The SP8853 contains a digital phase detector which feeds two charge pump circuits. Charge pump 1 has preset currents which are programmble as shown in Table 1. Charge pump 2 has a current level set by an external resistor RPD; the current is multiplied by a factor which is determined by bits G1 and G2 of the F1 or F2 word (see Table 1). Note that charge pump 2 current is pin 24 current × muliplication factor, where

$$\text{I pin 24} = \frac{V_{CC}-1{\cdot}5V}{RPD}$$

A lock detect circuit is connected to the output of charge pump 2. when the voltage level at pin 25 is between approximately 2·25V and 2·75V, LOCK DETECT (pin 27) will be low and charge pump 1 disabled, depending on the PD1 and PD2 programming bits as shown in Table 4.

The output signals from the *R* and *M* counters are available on pins 4 and 5 ($F_{PD}$ and $F_{REF}$) when programmed by the reference programming word; the various options are shown in Table 4. An external phase detector may be connected to pins 4 and 5 and may be used independently or in conjunction with the on-chip phase detector.

To allow for control direction changes introduced by the design of the control loop, a control bit in the F1/F2 programming word interchanges the inputs to the on-chip phase detector and reverses the functions on pins 4 and 5 (see Table 2).

| F1 or F2 word | | Charge pump 1 current (μA) | Charge pump 2 multiplier |
|---|---|---|---|
| G2 | G1 | | |
| 0 | 0 | 50 | 1 |
| 1 | 0 | 75 | 1·5 |
| 0 | 1 | 125 | 2·5 |
| 1 | 1 | 200 | 4 |

*Table 1 Charge pump currents*

| Output for RF phase lag | | | |
|---|---|---|---|
| F1/F2 sense bit | Pins 3 and 25 | Pin 4 | Pin 5 |
| 0 | Current source | $F_{PD}$ | $F_{REF}$ |
| 1 | Current sink | $F_{REF}$ | $F_{PD}$ |

*Table 2*

### Data Entry and Storage

The data section of the SP8853 consists of a data input interface, a data shift register and three data buffers.

Data is entered to the data input interface via a three-wire highway, with DATA (pin 24), CLOCK (pin 15) and ENABLE (pin16) inputs. The input interface routes the data into a 24-bit shift register with bus connections to three data buffers. Data entered via the serial bus is transferred to the appropriate data buffer on the negative transition of the data enable input according to the two final data bits C1 and C2 as shown in Table 3. The MSB of the data is entered first.

| 2-bit SR contents | | Buffer loaded |
|---|---|---|
| C2 | C1 | |
| 0 | 0 | F1 |
| 1 | 0 | F2 |
| 0 | 1 | Transfer A counter bits (N0:N3) into 4-bit buffer (see Figs. 2 and 7) |
| 1 | 1 | Reference |

*Table 3*

The dual F1/F2 buffer can receive two 22-bit words and controls the programmable divider A and M counters using 19 bits, the phase detector gain with two bits and the phase detector sense with one bit. A fourth input from the synthesiser control system selects the active buffer.

The third buffer contains only 16 bits, 13 being used to set the reference divider division ratio and 2 to control the phase detector enable logic. The remaining bit sets the dual modulus prescaler *N* ratio.

The data words may be entered in any individual multiple sequence and the shift register can be updated whils the data buffers retain control of the synthesiser with the previously loaded data. This enables four unique data words to be stored in the device, with three in the data buffers and a fourth in the shift register, while the chip is enabled. The F1 word may also be updated while F2 is controlling the programmable divider and vice-versa.

The dual F1/F2 buffer enables allows the device to be toggled between two frequencies using the F1/F2 select input at a rate determined by the comparison frequency and also permits random frequency hopping at a rate determined by a btye load period; this is possible because the loop can be locked to F1 while F2 is updated by entering new data via the shift register. The F1/F2 input is high to select F1.

An F1 or F2 update cycle will consist of a byte containing 24 bits whereas the reference byte will contain 18 bits. The device requires 3 bytes, each with a chip select sequence, totalling 66 bits to fully program.

When the dual modulus *A* counter is set to ÷8/9, the data required to set the counter is reduced by one bit, leaving an unused bit in the 22-bit F1/F2 buffer. This bit must always be set to zero when the ÷8/9 mode is required. Various programming sequences are shown in Fig. 7.

The data entry and storage registers are always powered up, making it possible to enter data when the device is in the powered down state.

| PD2 | PD2 | Result |
|---|---|---|
| 0 | 0 | $F_{REF}$ and $F_{PD}$ outputs off, charge pumps 1 and 2 on |
| 1 | 0 | $F_{REF}$ and $F_{PD}$ outputs on, charge pump 1 off, charge pump 2 on |
| 0 | 1 | $F_{REF}$ and $F_{PD}$ outputs off, charge pump 1 disabled by lock detect, charge pump 2 on |
| 1 | 1 | $F_{REF}$ and $F_{PD}$ outputs on, charge pump 1 disabled by lock detect, charge pump 2 on |

*Table 4*

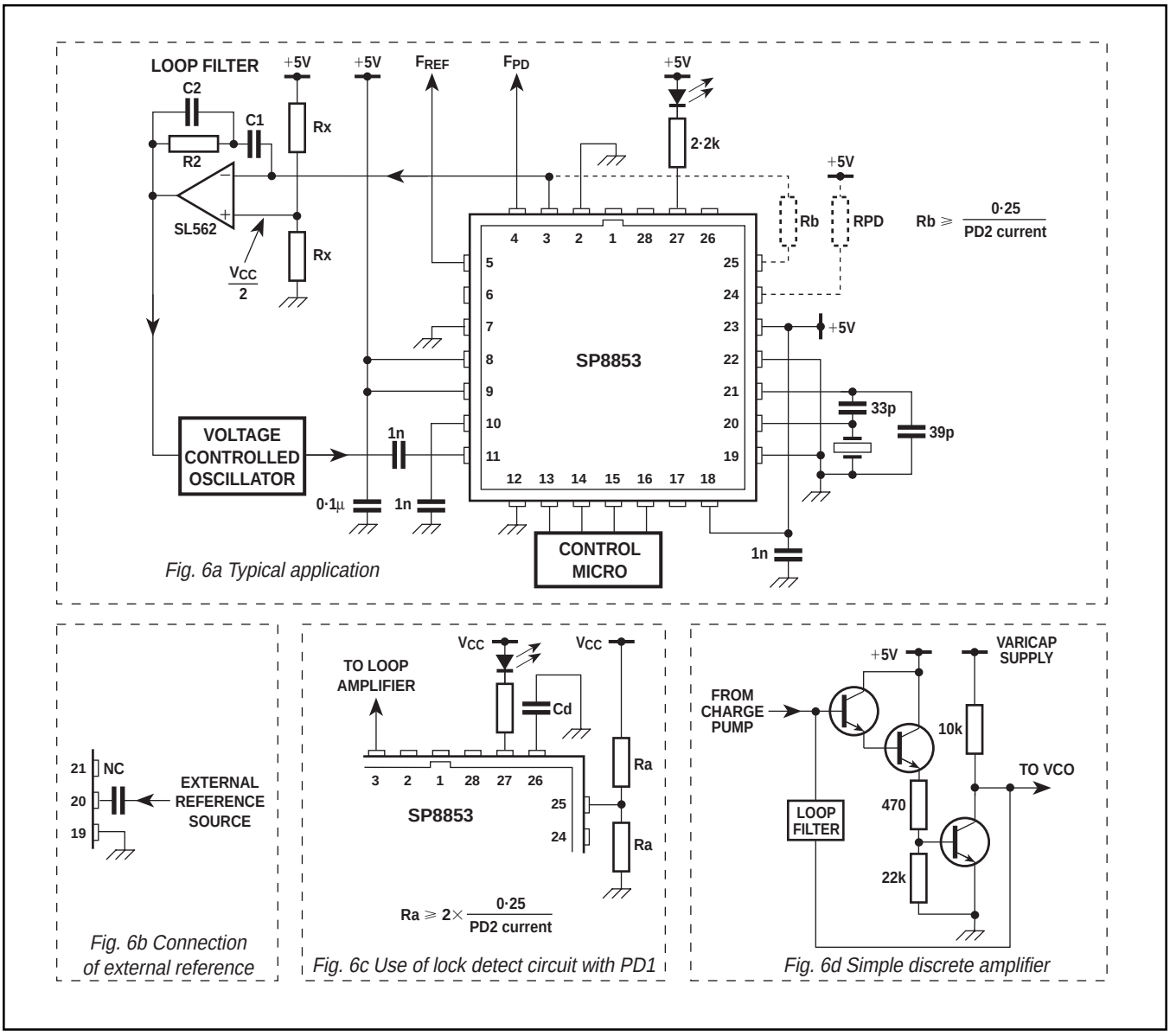



*Fig. 6a Typical application*

*Fig. 6b Connection of external reference*

*Fig. 6c Use of lock detect circuit with PD1*

*Fig. 6d Simple discrete amplifier*

*Fig. 6 Application diagrams*

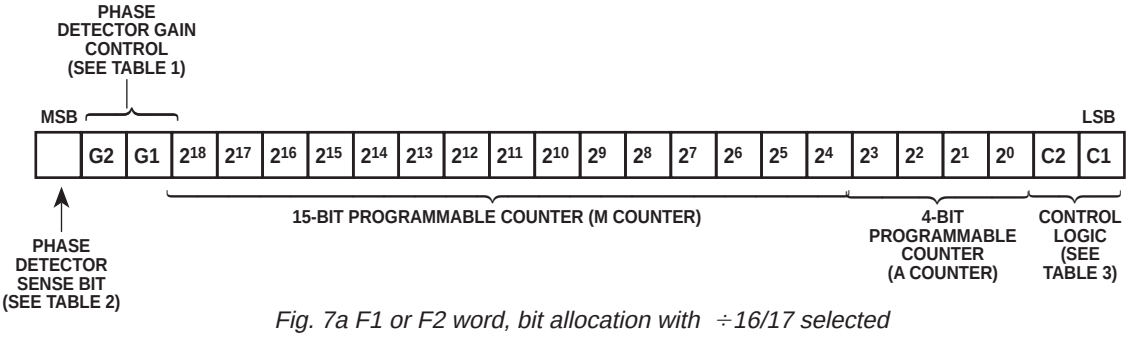



*Fig. 7a F1 or F2 word, bit allocation with ÷16/17 selected*

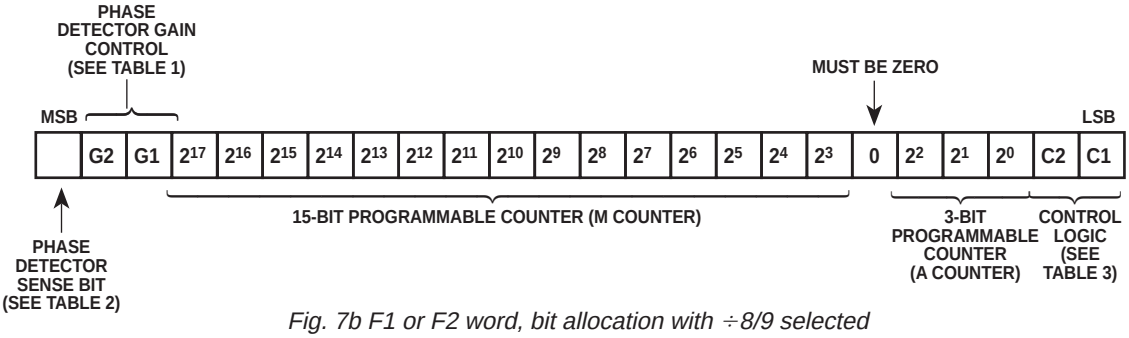



*Fig. 7b F1 or F2 word, bit allocation with ÷8/9 selected*

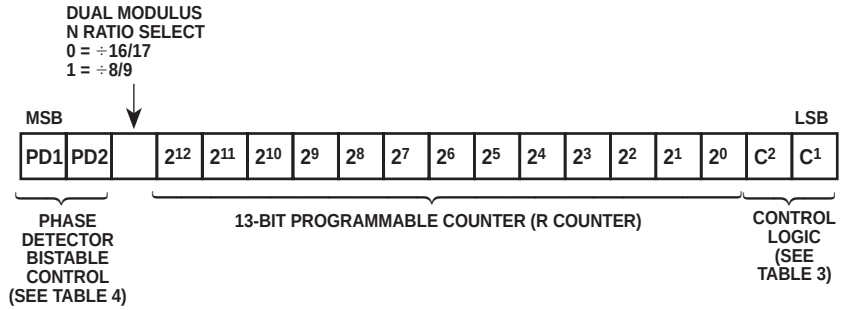



*Fig. 7c Reference word bit allocation*

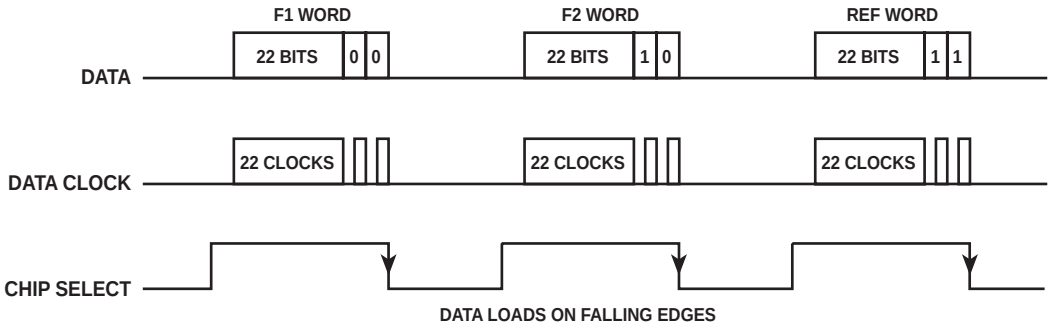



*Fig. 7d Data load sequence*

*Fig. 7 Data format diagrams*

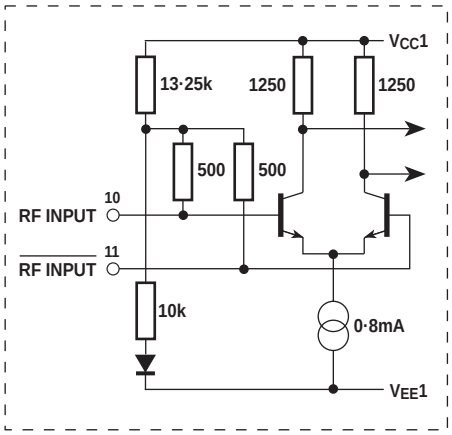



Fig. 8a RF preamplifer inputs

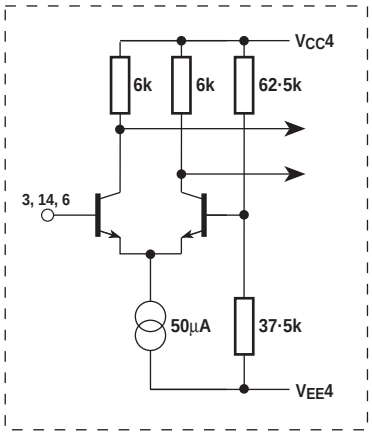



Fig. 8b F1/F2 data and power down inputs

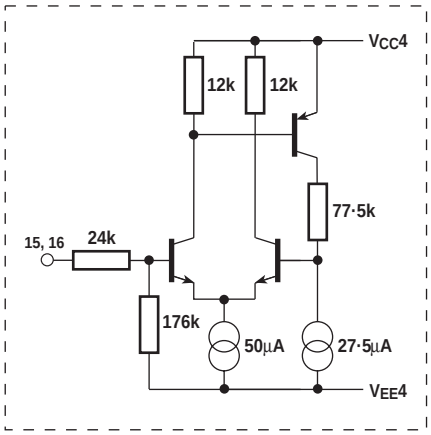



Fig. 8c Hysteresis inputs, data clock and enable

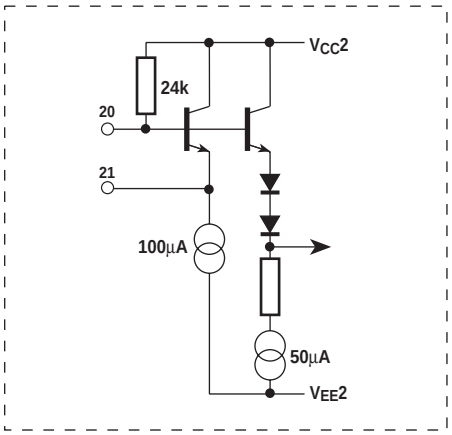



Fig. 8d Oscillator pins

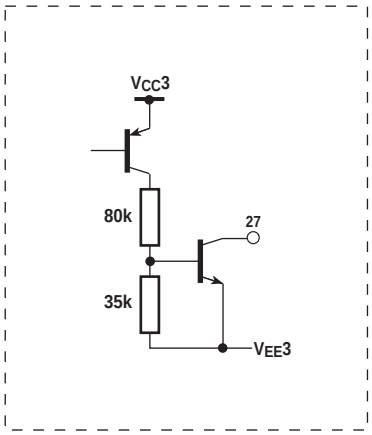



Fig. 8e Lock detect output

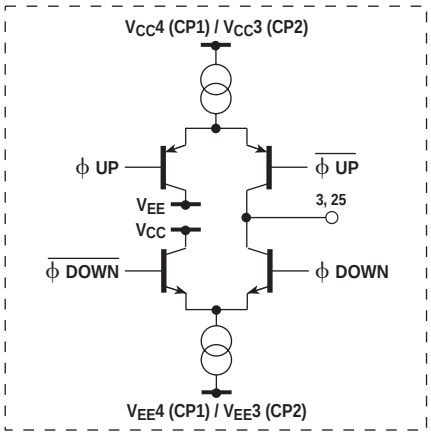



Fig. 8f Phase detector charge pumps

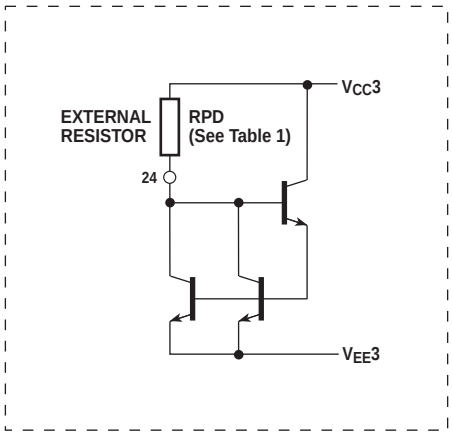



Fig. 8g Charge pump 2 current programming

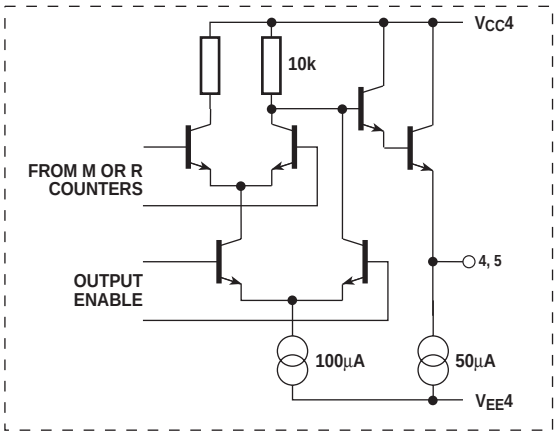



Fig. 8h $F_{PD}$ and $F_{REF}$ outputs

Fig. 8 Input and output interface diagrams

## DESCRIPTION

A basic application using a single phase detector is shown in Fig. 6a. The SP8853 is a 1·3GHz part so good RF design techniques should be employed, including the use of a ground plane and suitable high frequency capacitors at the RF input and for power supply decoupling.

The RF input should be coupled to either pin 10 or pin 11, with the other pin decoupled to ground. The reference oscillator is of conventional Colpitts type, with two capacitors required to provide a low impedance tap for the feedback signal to the transistor emitter. Typical values are shown in Fig. 6a, although these may be varied to suit the loading requirements of particular crystals. Where a suitable reference signal already exists or where a very stable source is required, it is possible to apply an external reference as shown in Fig. 6b. The amplitude should be kept below 0·5Vrms to avoid forward biasing the transistor's collector-base junction.

### Lock Detect and Charge Pump Operation

In some systems, it is useful to have an indication of phase lock. This function is provided on pin 27 (LOCK DETECT), which goes low when the output of charge pump 2 (PD2) is between 2·25V and 2·75V and can be used to drive an LED to give visual indication of phase lock. Alternatively, a pullup resistor may be connected from pin 27 to $V_{CC}$ and the output used to signal to the control microprocessor that the loop is locked, thus speeding up system operation. The output current available from pin 27 is limited to 1·5mA; if this is exceeded, the logic low level will be uncertain.

The circuit diagram of Fig. 6a is a basic application with minimum component count but which is neverthless perfectly adequate for many applications. Charge pump 1 output (pin3) is used to drive the loop amplifier which provides the control voltage for the VCO. When charge pump 1 is used in this mode, the PD1 and PD2 bits in the reference programming word must be set to enable charge pump 1 continuously (see Table 4). This application could also use charge pump 2 output (pin 25) or, if a higher phase detectot gain is required, pins 3 and 25 could be connected in parallel to use the combined output current from both charge pumps.

The lock detect circuit can be programmed to automatically disable charge pump 1 as shown in Table 4. This feature can be used to reduce the system lock up time by connecting the charge pump outputs in parallel to the loop amplifier with resistor Rb connected in series with charge pump 2 output. This connection allows a relatively high current to be used from charge pump 1 to give a short lock up time, and a low charge pump 2 current to be set to give low reference frequency sidebands. The degree of lock up time improvement depends on the ratio of charge pump 1 and charge pump 2 currents.

When the loop is out of lock, both charge pumps will be enabled and will feed current to the loop amplifier to bring the VCO to phase lock. The current from charge 2 will produce a voltage drop across Rb, allowing operation of the lock detect circuit and enabling charge pump 1. The value of Rb must be chosen to give a voltage drop greater than 0·25V at the current level programmed for charge pump 2. When phase lock is achieved, there will be no charge pump current and therefore the voltage at pin 25 will be equal to that on the virtual earth point of the loop amplifier (2·5V), disabling charge pump 1.

Charge pump 1 should not be left open circuit when enabled as this would prevent correct operation of the phase detector. The output on pin 3 should be biased to half supply with a pair of 4·7kΩ resistors connected across supplies.

When charge pump 2 is used to drive the loop amplifier, the lock detect circuit will only give an out of lock indication when large frequency changes are made or when a frequency outside the range of the VCO is programmed. at other times the loop amplifier is maintained at 2·5V by the action of the loop filter components. Again, a resistor connected between pin 25 and the loop amplifier, producing a voltage drop greater than 0·25V at the charge current programmed will allow sensitive out of lock detection.

When phase lock detection is required using charge pump 1 only, charge pump 2 output should be biased to 2·5V, using two equal value resistors, Ra, across the supply as shown in Fig. 6c. A small capacitor, Cd, connected frompin 28 to ground may be used to reduce chatter at the lock detect output. A detailed block diagram of the lock detect circuit is shown in Fig. 3.

### Choice of Loop Amplifier

The loop amplifier converts the charge pump current pulses into a voltage of a magnitude suitable for driving the chosen VCO. The choice of amplifier is determined by the voltage swing required at the VCO to achieve the necessary range. In most cases, an operational amplifier will be used to provide the essential characteristcs of high input impedance, high gain and low output impedance required in this application. A simple discrete design could also be used as shown in Fig. 6d. This arrangement can be particularly useful where the minimum VCO control voltage must be close to ground and where negative supplies are inconvenient. This form of amplifier is not suitable for use with charge pump 2 when the lock detect circuit is required.

When an operational amplifier is used in the inverting configuration shown in Fig. 6a, the charge pump output is connected directly to the virtual earth point and will therefore operate a a voltage close to that set on the non-inverting input. Normally, this operating point should be set at half supply using a potential divider of two equal value resistors, Rx, but if necessary the voltage can be set up to 1V higher or lower without detrimental effect. When the lock detect function is required on charge pump 2 however, the non-inverting input must be at half supply.

The digital phase detector and charge pump in the SP8853 produces bi-directional current pulses in order to correct errors between the reference and the VCO divider outputs. Once synchronisation is achieved, in theory no further output from the charge pump should be required. In practice, due to leakage currents and particularly the input current of the amplifier, the capacitors in the loop filter will gradually discharge, modifying the VCO control voltage and requiring further outputs from the charge pump to restore the charge. The effect of this continuous correction is to frequency modulate the VCO frequency and thus produce sidebands at the reference frequency. In order to reduce this effect to a minimum, an amplifier with low input bias is essential.

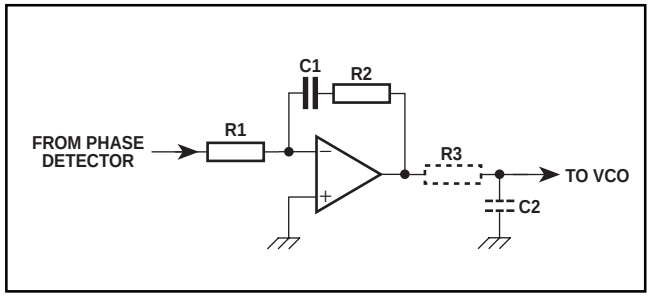



*Fig. 9 Standard form of second order loop filter*

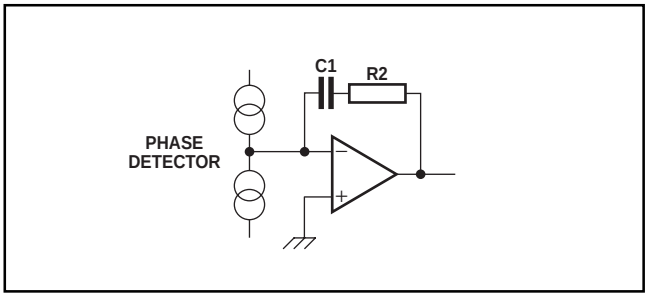



*Fig. 10 Modified form of second order loop filter*

## LOOP CALCULATIONS

Many frequency synthesiser designs use a second order loop with a loop filter of the form shown in Fig. 9.

In practice, an additional RC time constant (shown dashed in Fig. 9) is often added to reduce noise from the amplifier. In addition, any feedthrough capacitor or local decoupling at the VCO will be added to the value of $C_2$. These additional components in fact form a third order loop and, if the values are chosen correctly, the additional filtering provided can considerably reduce the level of reference frequency sidebands and noise without adversely affecting the loop settling time.

The calculations of values for both types of loop are shown below.

### Second Order Loop

For this filter, two equations are required to determine the time constants $\tau_1$ (= $C_1R_1$) and $\tau_2$ (= $C_1R_2$); the equations are:

$$\tau_1 = \frac{K_\theta K_0}{\omega_n^2 N} \quad \ldots(1)$$

$$\tau_2 = \frac{2\zeta}{\omega_n} \quad \ldots(2)$$

where

$K_\theta$ is the phase detector gain factor in V/radian
$K_0$ is the VCO gain factor = $2\pi\times10$MHz/V
$N$ is the division ratio from VCO to reference frequency
$\omega_n$ is the natural loop frequency = 500Hz
$\zeta$ is the damping factor = 0·7071

The SP8853 phase detector is a current source rather than a conventional voltage source and has a gain factor specified in μA/radian. Since the equations deal with a filter where $R_1$ is feeding the virtual earth point of an operational amplifier from a voltage source, $R_1$ sets the input current to the filter – similar to the circuit shown in Fig. 10 – where a current source phase detector is connected directly to the virtual earth point of the operational amplifier.

The equivalent voltage gain of the phase detector can be calculated by assuming a value for $R_1$ and calculating a gain in V/radian which would produce the set current.

The digital phase detector used in the SP8853 is linear over a range of $2\pi$ radians and therefore the phase detector gain is given by:

$$K_\theta = \frac{\text{Phase detector current setting}}{2\pi}\ \mu\text{A/radian}$$

For $R_1$ = 1kΩ and assuming a value of phase detector current of 50μA, the phase detector gain is therefore:

$$K_\theta = \frac{50\mu A}{2\pi}\times10^3$$

$$= \mathbf{0{\cdot}00796V/radian}$$

This value can now be inserted in equation 1 to obtain a value for $C_1$ and equation 2 used to determine a value for $R_2$.

**Example**

Calculate values for a second order loop with the following parameters:

Frequency to be synthesised = 800MHz
Reference frequency =100kHz

Division ration $N$ $= \frac{800\text{MHz}}{100\text{kHz}}$

$= \mathbf{8000}$

From equation (1), $\tau_1 = \frac{0{\cdot}0796\times2\pi\times10^6}{(2\pi\times500)^2\times8\times10^3}$

$\therefore \tau_1 = \mathbf{6{\cdot}334\mu s}$

From equation (2), $\tau_2 = \frac{2\times0{\cdot}7071}{2\pi\times500}$

$\therefore \tau_2 = \mathbf{450\mu s}$

Now, since $\tau_1 = C_1R_1$, $C_1 = \frac{6{\cdot}334\times10^{-6}}{10^3}$

$\therefore C_1 = \mathbf{6{\cdot}33nF}$

and, since $\tau_2 = C_1R_2$, $R_2 = \frac{4{\cdot}5\times10^{-4}}{6{\cdot}33\times10^{-9}}$

$\therefore R_2 = \mathbf{71k\Omega}$

### Third Order Loop

The third order loop is normally as shown in Fig. 11. Fig. 12 shows the circuit redrawn to use an RC time constant after the amplifier, allowing any feedthrough capacitance on the VCO line to be included in the loop calculations. Where the modified form in Fig. 12 is used, it is advantageous to connect a small capacitor $C_X$ of typically 100pF (shown dashed) across $R_2$ to reduce sidebands caused by the amplifier being forced into non-linear operation by the phase comparator pulses

Three equations are required to determine the time constants $\tau_1$, $\tau_2$, and $\tau_3$, where

for Fig. 11
$\tau_1 = C_1R_1$
$\tau_2 = R_2(C_1+C_2)$
$\tau_3 = C_2R_2$

and for Fig. 12
$\tau_1 = C_1R_1$
$\tau_2 = C_1R_2$
$\tau_3 = C_2R_3$

The equations are:

$$\tau_1 = \frac{K_\theta K_0}{\omega_n^2 N}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{\frac{1}{2}} \quad \ldots(3)$$

$$\tau_2 = \frac{1}{\omega_n^2\tau_3^2} \quad \ldots(4)$$

$$\tau_3 = \frac{-\tan\Phi_0 + \frac{1}{\cos\Phi_0}}{\omega_n} \quad \ldots(5)$$

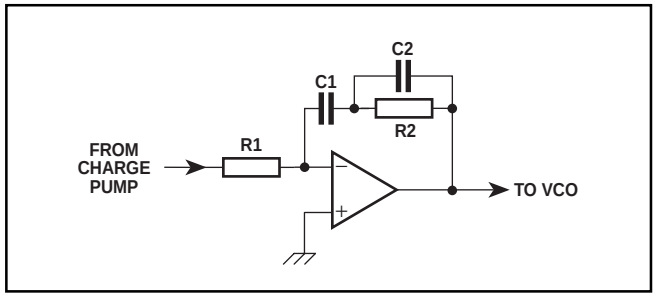



*Fig. 11 Standard form of third order loop filter*

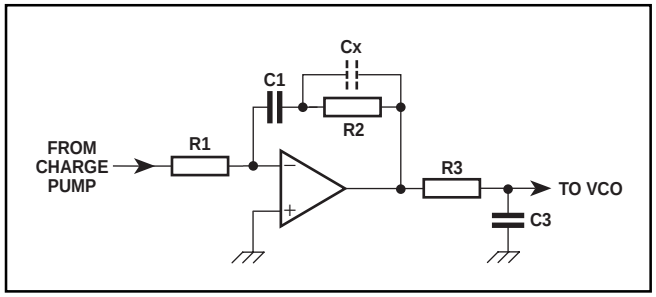



*Fig. 12 Modified form of third order loop filter*

where $K_\theta$, $K_0$, $N$ and $\omega_n$ are as defined for the second order loop and $\Phi_0$ is the phase margin, normally set to 45°. These values can now be substituted in equation (3) to obtain a value for $C_1$ and in equations (4) and (5) to determine values for $C_2$ and $R_2$.

Example

Calculate values for a third order loop with parameters as for the second order loop and $\Phi_0 = 45°$.

From equation (5):

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{500\text{Hz} \times 2\pi}$$

$$= \frac{0{\cdot}4142}{3161{\cdot}6}$$

$$\therefore \tau_3 = \mathbf{131{\cdot}8\mu s}$$

From equation (4):

$$\tau_2 = \frac{1}{(500 \times 2 \times \pi)^2 \times 1{\cdot}318 \times 10^{-4}}$$

$$\therefore \tau_2 = \mathbf{768{\cdot}7\mu s}$$

Using these values in equation (3):

$$\tau_1 = \frac{7{\cdot}96 \times 10^{-3} \times 2\pi \times 10\text{MHz/V}}{8000 \times (500 \times 2\pi)^2} \times [A]^{\frac{1}{2}}$$

$$\text{where A} = \left[\frac{1 + \omega_n^2 \tau_2^2}{1 + \omega_n^2 \tau_3^2}\right]$$

$$= \frac{1 + (500 \times 2\pi)^2 \times (7{\cdot}687 \times 10^{-4})^2}{1 + (500 \times 2\pi)^2 \times (1{\cdot}318 \times 10^{-4})^2}$$

$$\tau_1 = \frac{500141{\cdot}6}{7{\cdot}896 + 10^{10}} \left[\frac{6{\cdot}832}{1{\cdot}1714}\right]^{\frac{1}{2}}$$

$$= 6{\cdot}334 \times 10^{-6} \times 2{\cdot}415$$

$$\therefore \tau_1 = \mathbf{15{\cdot}3\mu s}$$

Now, since $\tau_1 = C_1 R_1$ and $R_1 = 1\text{k}\Omega$, $C_1 = \frac{1{\cdot}53 \times 10^{-5}}{10^3}$

$$\therefore C_1 = \mathbf{0{\cdot}0153\mu F}$$

For Fig. 11, $\tau_2 = R_2 (C_1 + C_2)$

For Fig. 12, $\tau_3 = C_2 R_2$

Substituting for $C_2$:

$$\tau_2 = R_2 \left[C_1 + \frac{\tau_3}{R_2}\right] = R_2 C_1 + \tau_3$$

$$\text{or, } R_2 = \frac{\tau_2 - \tau_3}{C_1}$$

$$= \frac{7{\cdot}687 \times 10^{-4} - 1{\cdot}318 \times 10^{-4}}{0{\cdot}0153 \times 10^{-6}}$$

$$\therefore R_2 = \mathbf{41{\cdot}627k\Omega}$$

$$\tau_3 = C_2 R_2 = \frac{\tau_3}{R_2}$$

$$= \frac{1{\cdot}318 \times 10^{-4}}{41627}$$

$$\therefore C_2 = \mathbf{3{\cdot}17nF}$$

For Fig. 12, $\tau_1 = C_1 R_1$

$$\text{or, } C_1 = \frac{1{\cdot}53 \times 10^{-5}}{10^3}$$

$$\therefore C_1 = \mathbf{0{\cdot}0153nF}$$

$$\tau_2 = C_1 R_2$$

$$\text{or, } R_2 = \frac{7{\cdot}687 \times 10^{-4}}{1{\cdot}53 \times 10^{-8}}$$

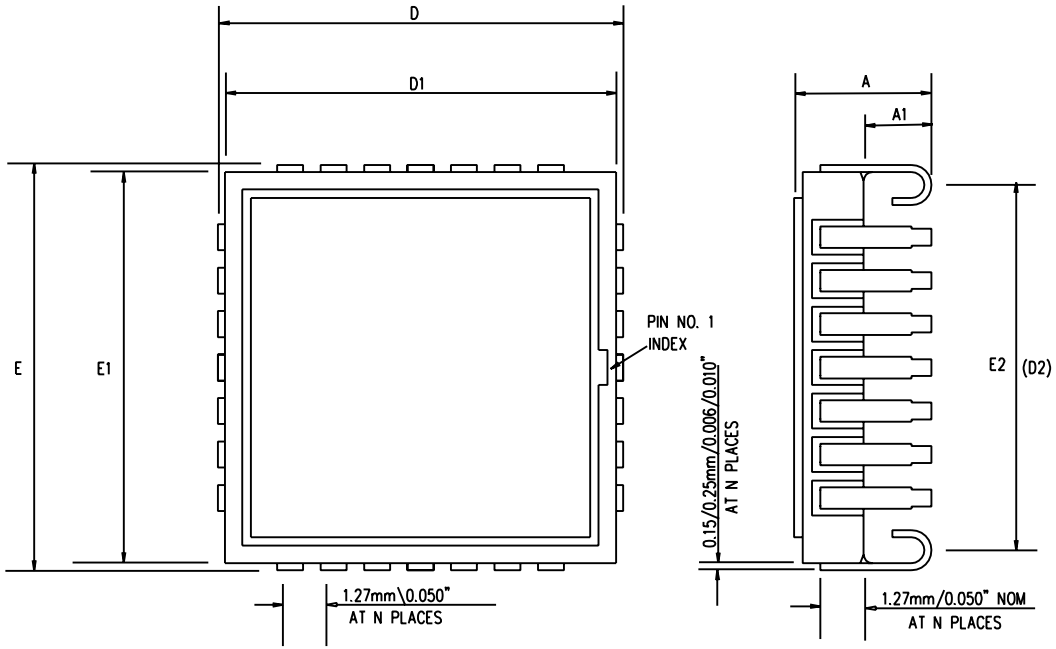
$$\therefore R_2 = \mathbf{50{\cdot}242k\Omega}$$

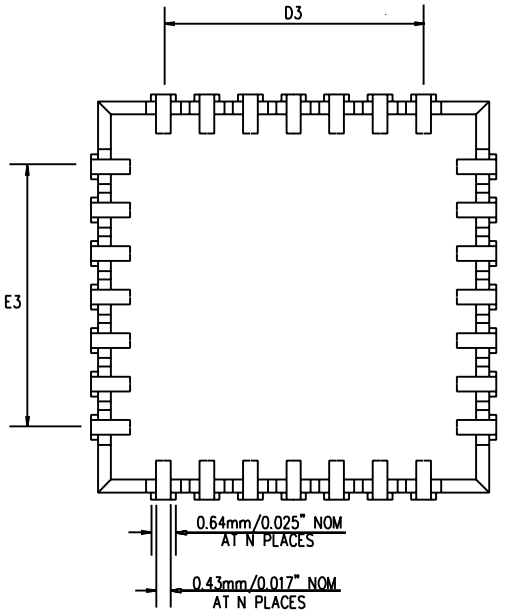
$$\tau_3 = C_2 R_3$$

Since the values of $C_2$ and $R_3$ are independent of the other components, either can be chosen and the other determined. Assuming that $R_3 = 1\text{k}\Omega$, then

$$C_2 = \frac{1{\cdot}318 \times 10^{-4}}{10^3}$$

$$\therefore C_2 = \mathbf{0{\cdot}01318\mu F}$$




| Symbol | Altern. Dimensions in millimetres | | | Control Dimensions in inches | |
|---|---|---|---|---|---|
| | MIN | MAX | | MIN | MAX |
| A | 3.94 | 4.11 | | 0.155 | 0.162 |
| A1 | 1.98 | | | 0.078 | |
| D | 11.73 | | | 0.461 | |
| D1 | 11.18 | 11.68 | | 0.440 | 0.460 |
| D2 | 10.16 | 11.18 | | 0.400 | 0.440 |
| D3 | 7.37 | 7.87 | | 0.290 | 0.310 |
| E | 11.73 | | | 0.461 | |
| E1 | 11.18 | 11.68 | | 0.400 | 0.460 |
| E2 | 10.16 | 11.18 | | 0.400 | 0.440 |
| E3 | 7.37 | 7.87 | | 0.290 | 0.310 |
| | Pin features | | | | |
| N | 28 | | | | |
| ND | 7 | | | | |
| NE | 7 | | | | |
| NOTE | SQUARE | | | | |

Note:-
1. This drawing supersedes 418/ED/51186/001 issue 2



| | | | | |
|---|---|---|---|---|
| ISSUE | 1 | 2 | | |
| ACN | 207466 | 212488 | | |
| DATE | 10Sep99 | 8Apr02 | | |
| APPRD. | | | | |

ZARLINK SEMICONDUCTOR

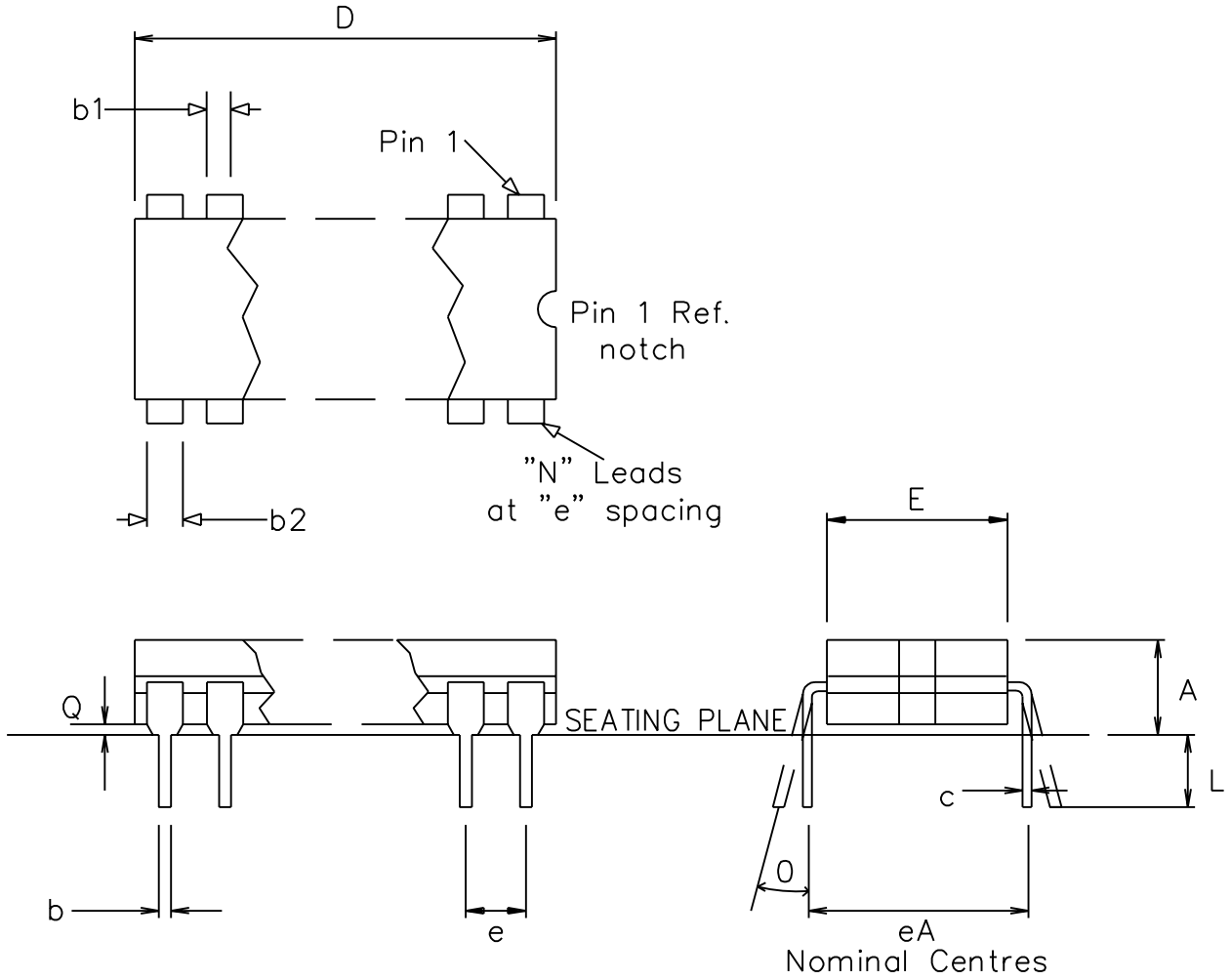
Previous package codes

HC / J

Package Code QF

Package Outline for
28 lead J-LDCC

GPD00602




| Symbol | Altern. Dimensions in millimetres | | | | Control Dimensions in inches | | |
|---|---|---|---|---|---|---|---|
| | MIN | Nominal | MAX | | MIN | Nominal | MAX |
| L | 3.18 | | 4.06 | | 0.125 | | 0.160 |
| A | | | 5.59 | | | | 0.220 |
| Q | 0.51 | | | | 0.020 | | |
| E | 12.70 | | 15.49 | | 0.500 | | 0.610 |
| eA | | 15.24 | | | | 0.600 | |
| c | 0.20 | | 0.36 | | 0.008 | | 0.014 |
| D | | | 38.10 | | | | 1.500 |
| e | 2.54 BSC. | | | | 0.100 BSC. | | |
| b1 | 1.14 | | 1.65 | | 0.045 | | 0.065 |
| b | 0.36 | | 0.58 | | 0.014 | | 0.023 |
| b2 | 0.73 | | 1.12 | | 0.029 | | 0.044 |
| 0 | | | 15° | | | | 15° |
| | | | | | | | |
| | Pin features | | | | | | |
| N | 28 | | | | | | |
| ND | 14 | | | | | | |
| NE | 0 | | | | | | |
| NOTE | RECTANGULAR | | | | | | |

This drawing supersedes 418/ED/39501/009 (Swindon)



| ISSUE | 1 | 2 | | |
|---|---|---|---|---|
| ACN | 201736 | 212462 | | |
| DATE | 20Nov96 | 27Mar02 | | |
| APPRD. | | | | |

ZARLINK SEMICONDUCTOR

Previous package codes

DG / C

Package Code DH

Package Outline for 28 lead DIL (Glass Seal Ceramic)

GPD00281

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**www.zarlink.com**